

FORM PTO-1449
(REV. 6-89)

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

Attorney's Docket No.

16787-06114

Serial No.

09/922,371

INFORMATION DISCLOSURE CITATION

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Applicant

Ajay Naini et al.

Filing Date

August 2, 2001

Group Art Unit

Unassigned

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

mm	Q	Robert E. Goldschmidt, "Applications of Division by Convergence", <i>Paper submitted for Master of Science Degree, Massachusetts Institute of Technology</i> , June, 1964, pgs. 1-44
	R	American National Standard, "IEEE Standard for Binary Floating-Point Arithmetic", <i>IEEE Standard 754</i> , 1985, pgs. 1-14
	S	Israel Koren, "Computer Arithmetic Algorithms", <i>Binary Floating-Point Numbers, Fast Addition</i> , Chapters 4, 5, 1993, pgs. 45-98
	T	SPARC International, Inc., "The SPARC Architecture Manual, Version 9", 1993

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<div style="font-family: cursive; font-size: 1.2em;">man</div>	<div style="display: flex;"> <div style="width: 20px; text-align: center; font-weight: bold;">F</div> <div>Stuart F. Oberman and Michael J. Flynn, "Division Algorithms and Implementations", <i>IEEE Transactions on Computers</i>, Vol. 46, No. 8, August 1997, pp. 833-854.</div> </div> <div style="display: flex;"> <div style="width: 20px; text-align: center; font-weight: bold;">G</div> <div>C.V. Ramamoorthy et al., "Some Properties of Iterative Square-Rooting Methods Using High-Speed Multiplication", <i>IEEE Transactions on Computers</i>, Vol. c-21, No. 8, August 1972, pp. 837-847.</div> </div> <div style="display: flex;"> <div style="width: 20px; text-align: center; font-weight: bold;">H</div> <div>E. M. Schwartz, et al., "CMOS Floating-Point Unit for the S/390 Parallel Enterprise Server G4", <i>IBM Journal of Research & Development</i>, Vol. 41, No. 4/5, pp. 1-17, April 10, 2001.</div> </div> <div style="display: flex;"> <div style="width: 20px; text-align: center; font-weight: bold;">I</div> <div>Michael J. Schulte and Earl E. Swartzlander, Jr., "A Family of Variable-Precision Interval Arithmetic Processors", <i>IEEE Transactions on Computers</i>, Vol. 49, No. 5, pp. 1-11, May 2000.</div> </div> <div style="display: flex;"> <div style="width: 20px; text-align: center; font-weight: bold;">J</div> <div>Andrew D. Booth, "A Signed Binary Multiplication Technique", <i>Quart. Journ. Mech. and Applied Math.</i>, Vol. IV, Pt. 2, pp. 236-240.</div> </div> <div style="display: flex;"> <div style="width: 20px; text-align: center; font-weight: bold;">K</div> <div>Christopher Williard, "Superdome - Hewlett-Packard Extends its High-End Computing Capabilities", <i>IDC</i>, pp. 1-20, 2000.</div> </div> <div style="display: flex;"> <div style="width: 20px; text-align: center; font-weight: bold;">L</div> <div>Eric M. Schwartz, "Rounding for Quadratically Converging Algorithms for Division and Square Root", <i>Conference Record of The Twenty-Ninth Asilomar Conference on Signals, Systems and Computers</i>, pp. 600-603, October 30, 1995.</div> </div> <div style="display: flex;"> <div style="width: 20px; text-align: center; font-weight: bold;">M</div> <div>Debjit Das Sarma and David W. Matula, "Measuring the Accuracy of ROM Reciprocal Tables", <i>11th Symposium on Computer Arithmetic</i>, pp. 95-102, June 29, 1993.</div> </div> <div style="display: flex;"> <div style="width: 20px; text-align: center; font-weight: bold;">N</div> <div>Robert K. Yu and George B. Zyner, "167 MHz-4 Floating Point Multiplier", <i>12th Symposium on Computer Arithmetic</i>, pp. 149-154, July 19, 1995.</div> </div> <div style="display: flex;"> <div style="width: 20px; text-align: center; font-weight: bold;">O</div> <div>Mark R. Santoro, et al., "Rounding Algorithms for IEEE Multipliers", <i>Proceedings, 9th Symposium on Computer Arithmetic</i>, pp. 176-183.</div> </div> <div style="display: flex;"> <div style="width: 20px; text-align: center; font-weight: bold;">P</div> <div>C. S. Wallace, "A Suggestion for a Fast Multiplier", <i>IEEE Transactions on Electronic Computers</i>, pp. 14-17, February 1964.</div> </div>

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Man	A	E. Hokenek, et al., "Leading-zero anticipator (LZA) in the IBM RISC System/6000 Floating Point Execution Unit", IBM J. Res. Develop., Vol. 34, No. 1, January 1990
I	B	Hiroaki Suzuki et al., "Leading-Zero Anticipatory Logic for High-Speed Floating Point Addition", IEEE Journal of Solid-State Circuits, Vol. 31, No. 8, August 1996
	C	Nhon T. Quach, et al., "An Improved Algorithm for High-Speed Floating-Point Addition", Technical Report: CSL-TR-90-442, August 1990
	D	A. Beaumont-Smith et al., "Reduced Latency IEEE Floating-Point Standard Adder Architectures", Department of Electrical and Electronic Engineering, University of Adelaide, Australia, August 1999, pgs. 35-42
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